FIGURE 1 (Prior Art)

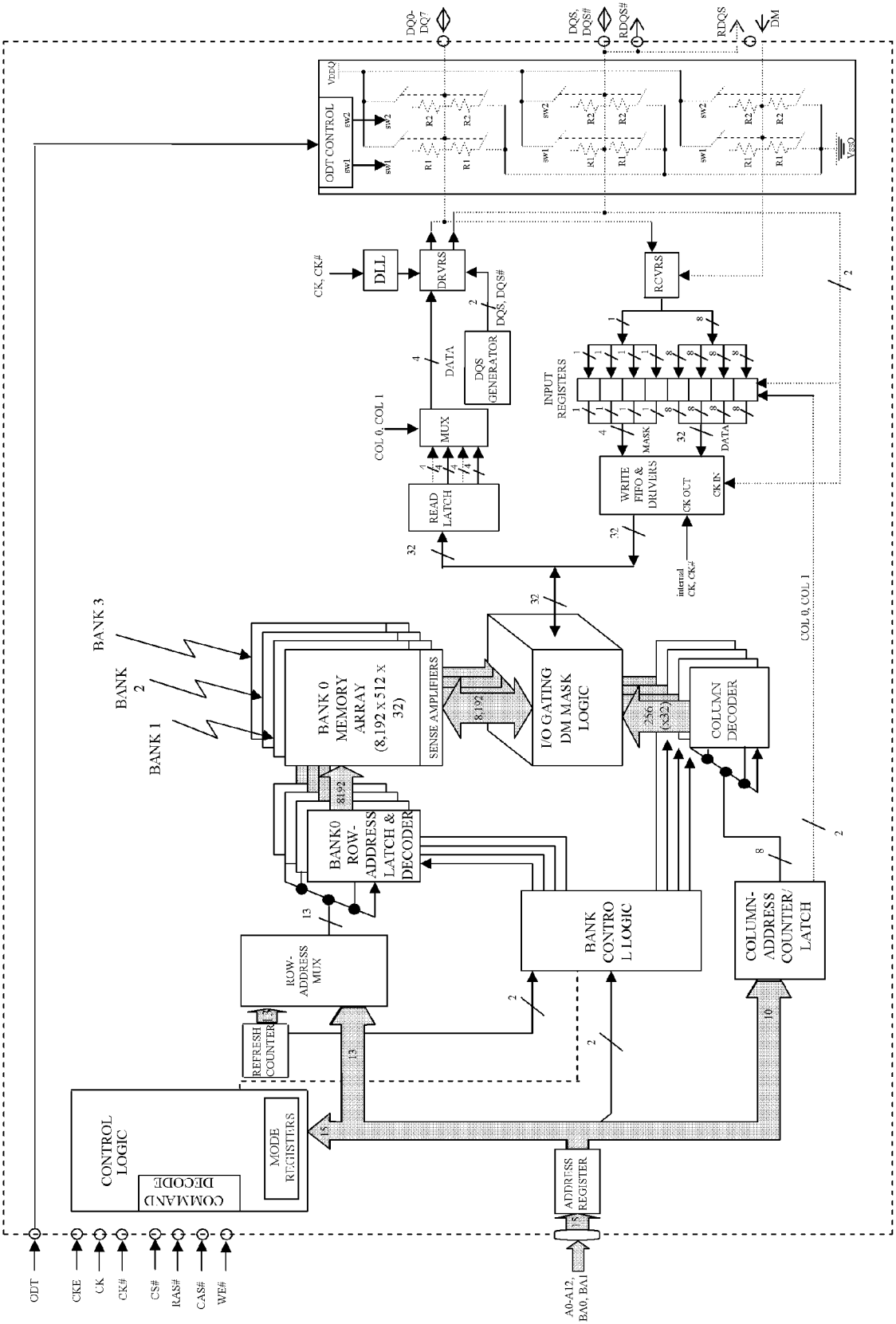


FIGURE 2 (Prior Art)

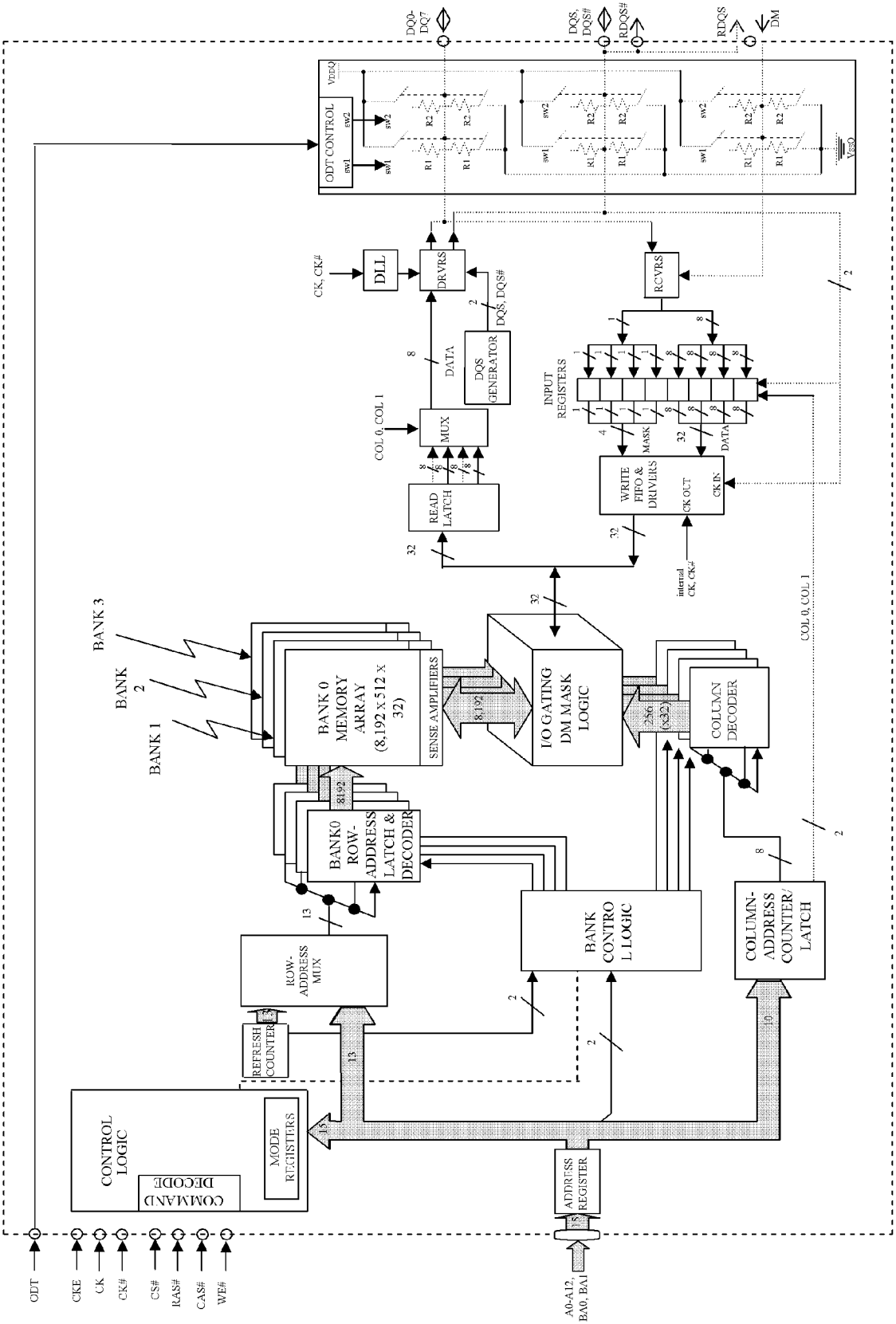
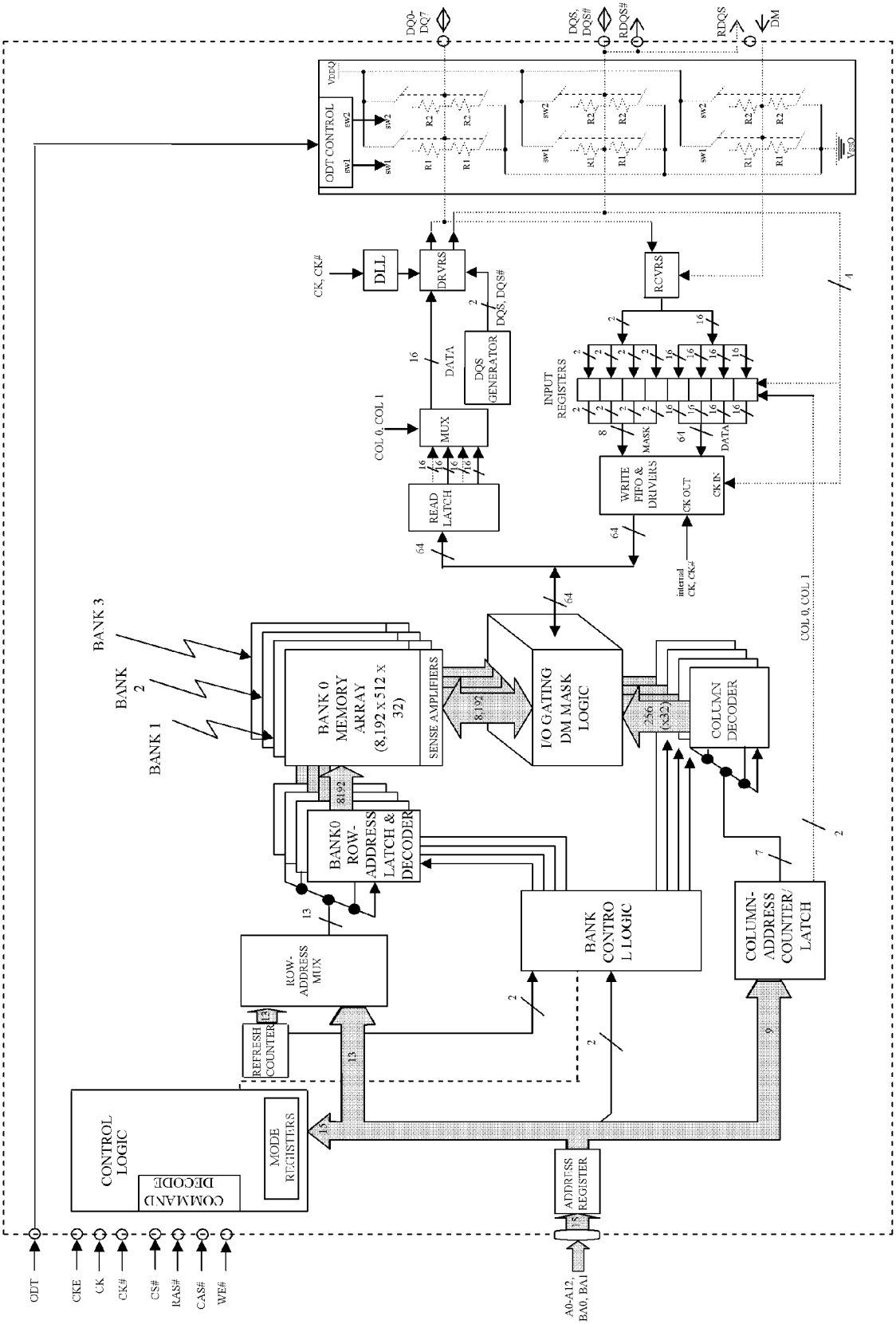


FIGURE 3 (Prior Art)



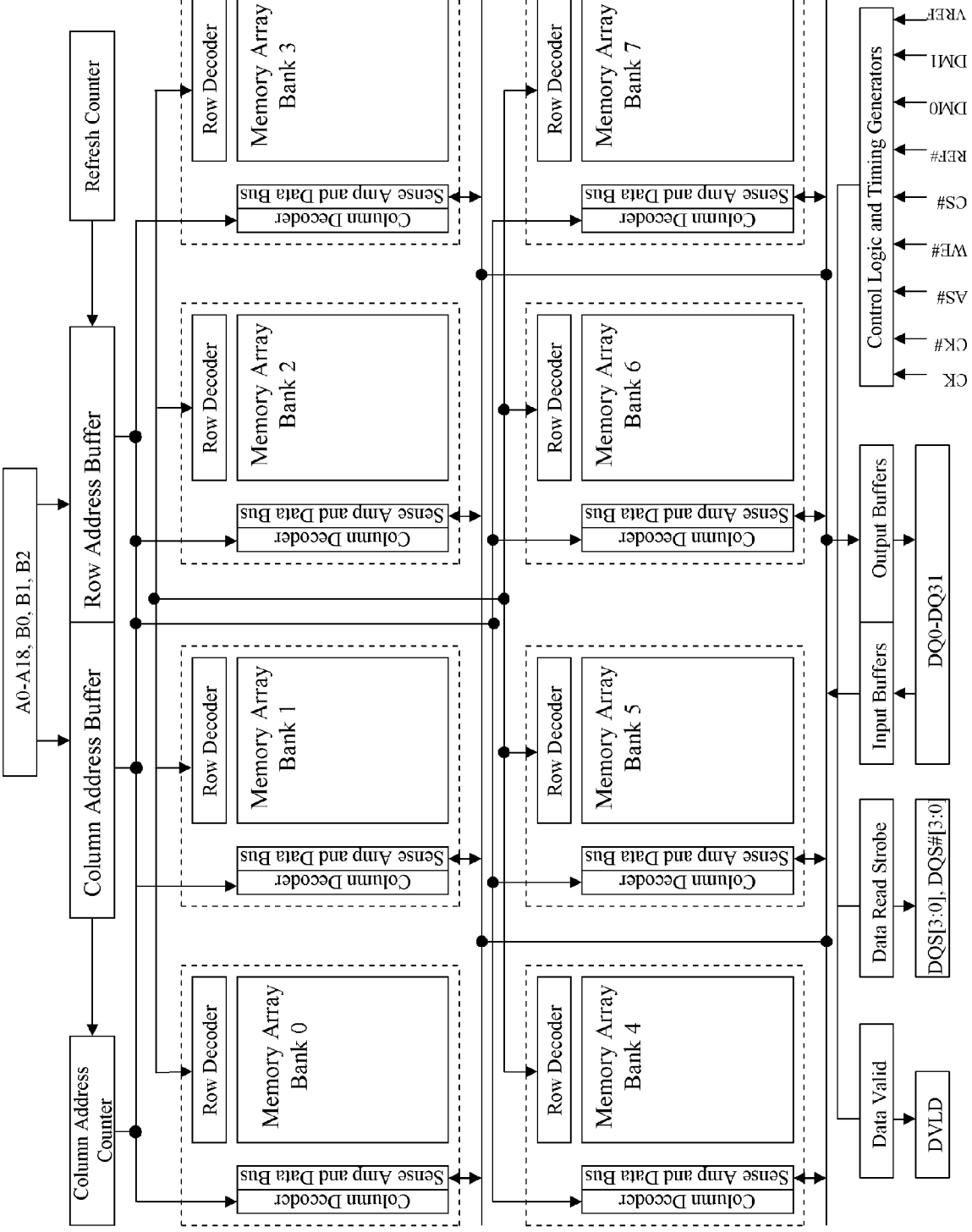
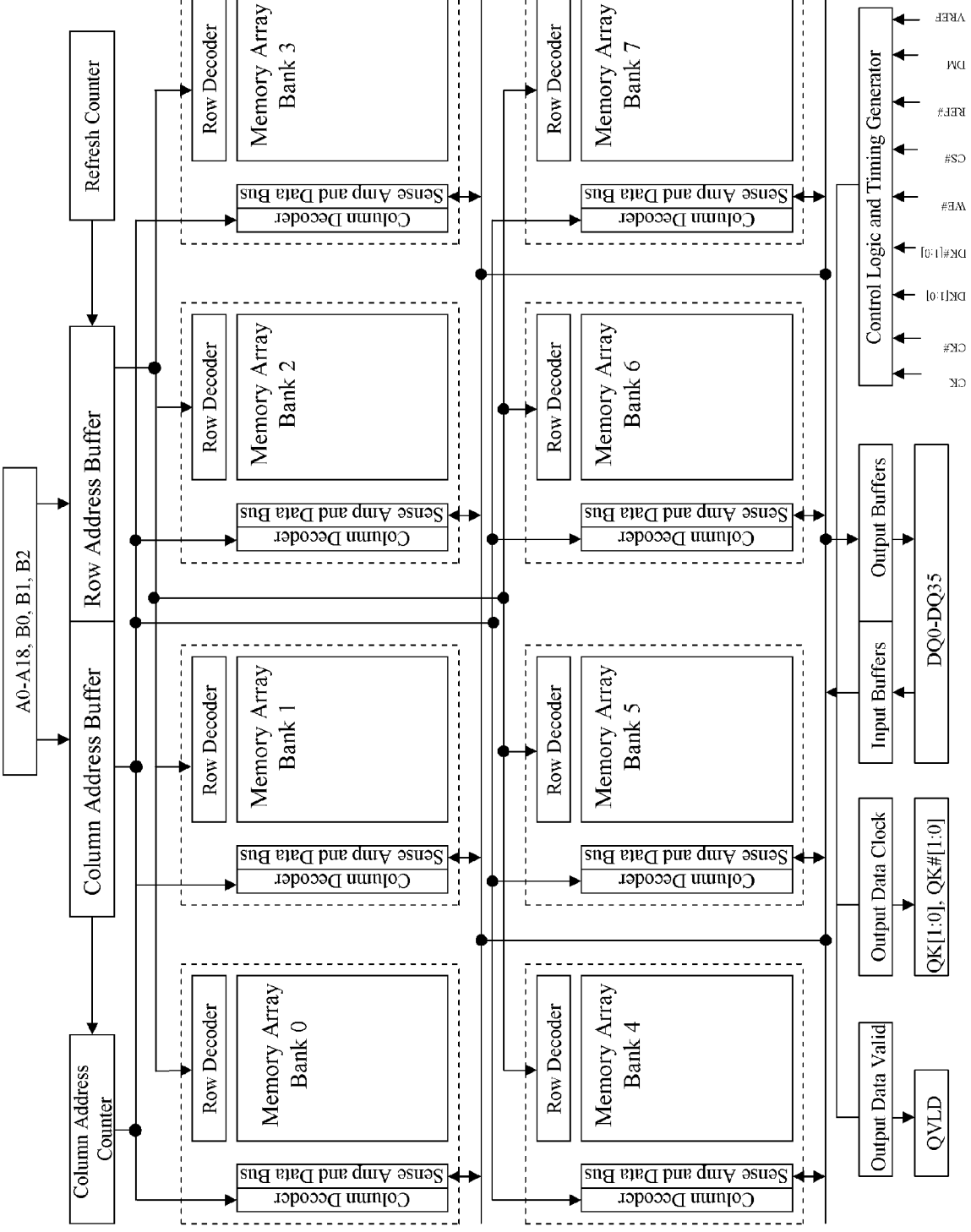


FIGURE 4
(Prior Art)

FIGURE 5
(Prior Art)



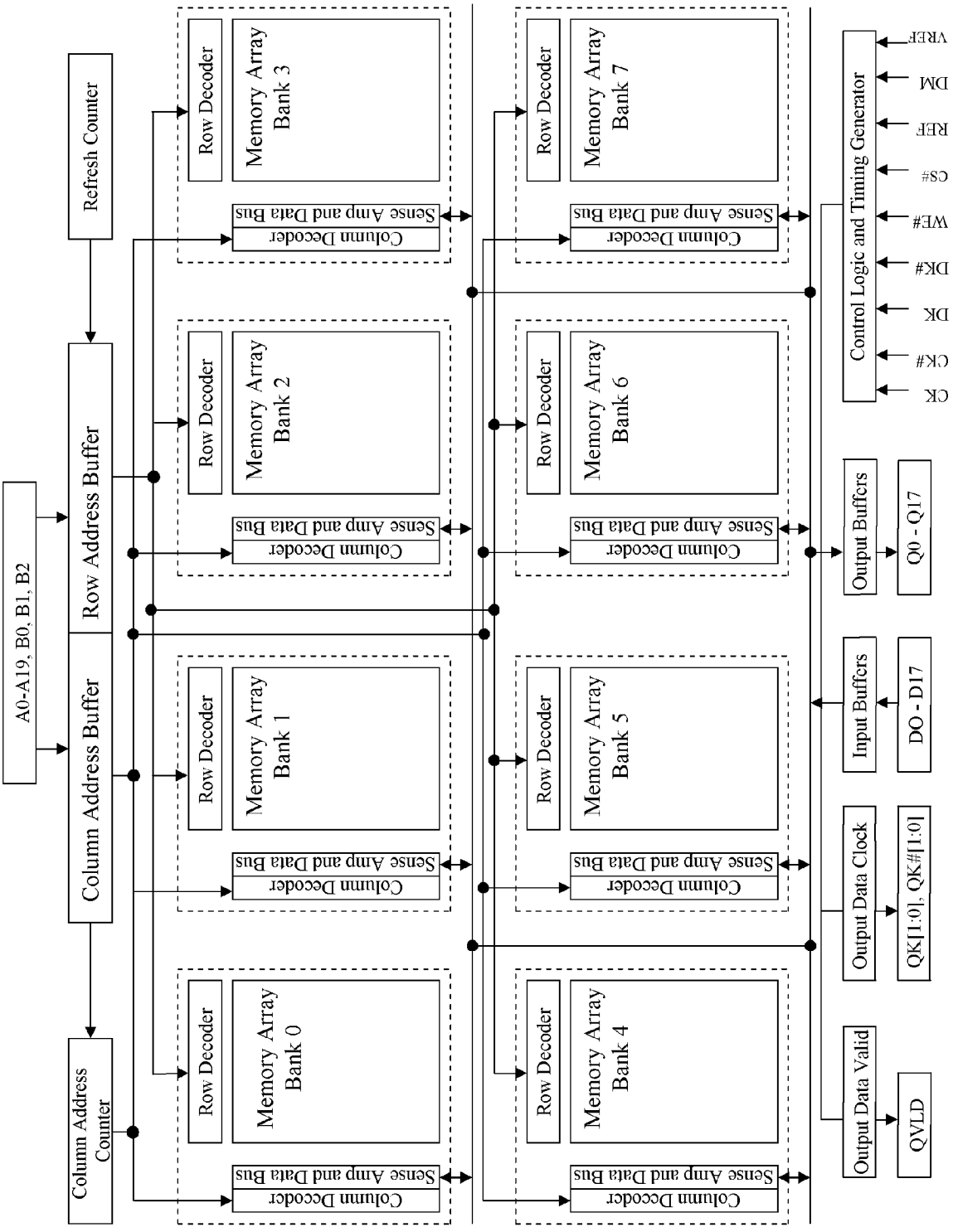


FIGURE 6
(Prior Art)

FIGURE 7

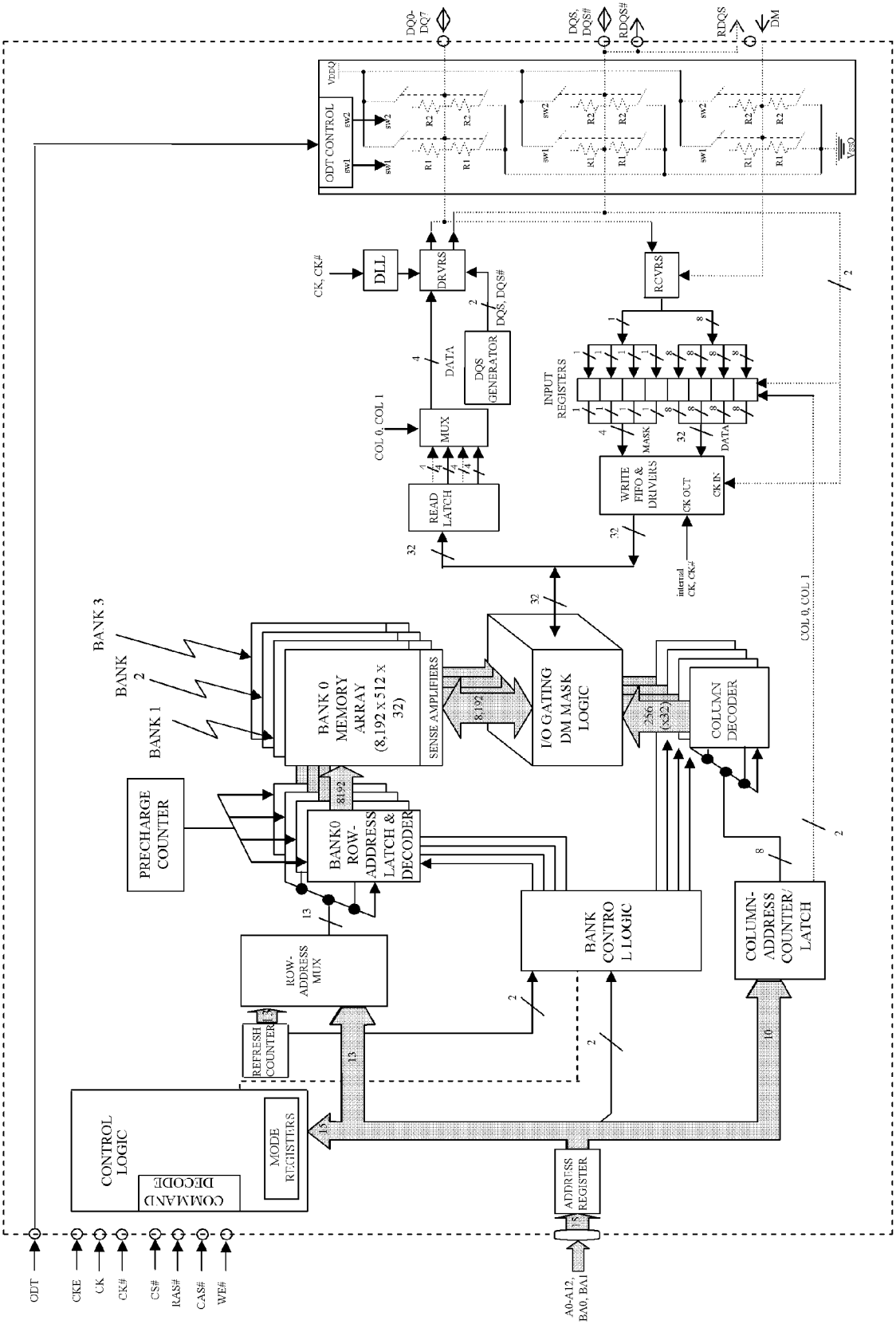

ODT
CKE
CK
CK#
CS#
RAS#
CAS#
WE#
A0-A12, BA0, BA1
CONTROL LOGIC
COMMAND DECODE
MODE REGISTERS
REFRESH COUNTER
ROW-ADDRESS MUX
ADDRESS REGISTER
BANK CONTROL LOGIC
COLUMN-ADDRESS COUNTER/ LATCH
PRECHARGE COUNTER
BANK0 ROW-ADDRESS LATCH & DECODER
BANK 3
BANK 2
BANK 1
BANK 0 MEMORY ARRAY (8,192 x 512 x 32)
SENSE AMPLIFIERS
I/O GATING DM MASK LOGIC
COLUMN DECODER
COL 0, COL 1
READ LATCH
MUX
DATA
DQS GENERATOR
DLL
DRVRS
RCVRS
WRITE FIFO & DRIVERS
INPUT REGISTERS
MASK
DATA
CK OUT
CKIN
internal CK, CK#
CK, CK#
DQS, DQS#
DQ0-DQ7
RDQS#
RDQS
DM
ODT CONTROL
VDDQ
VSSQ

FIGURE 8

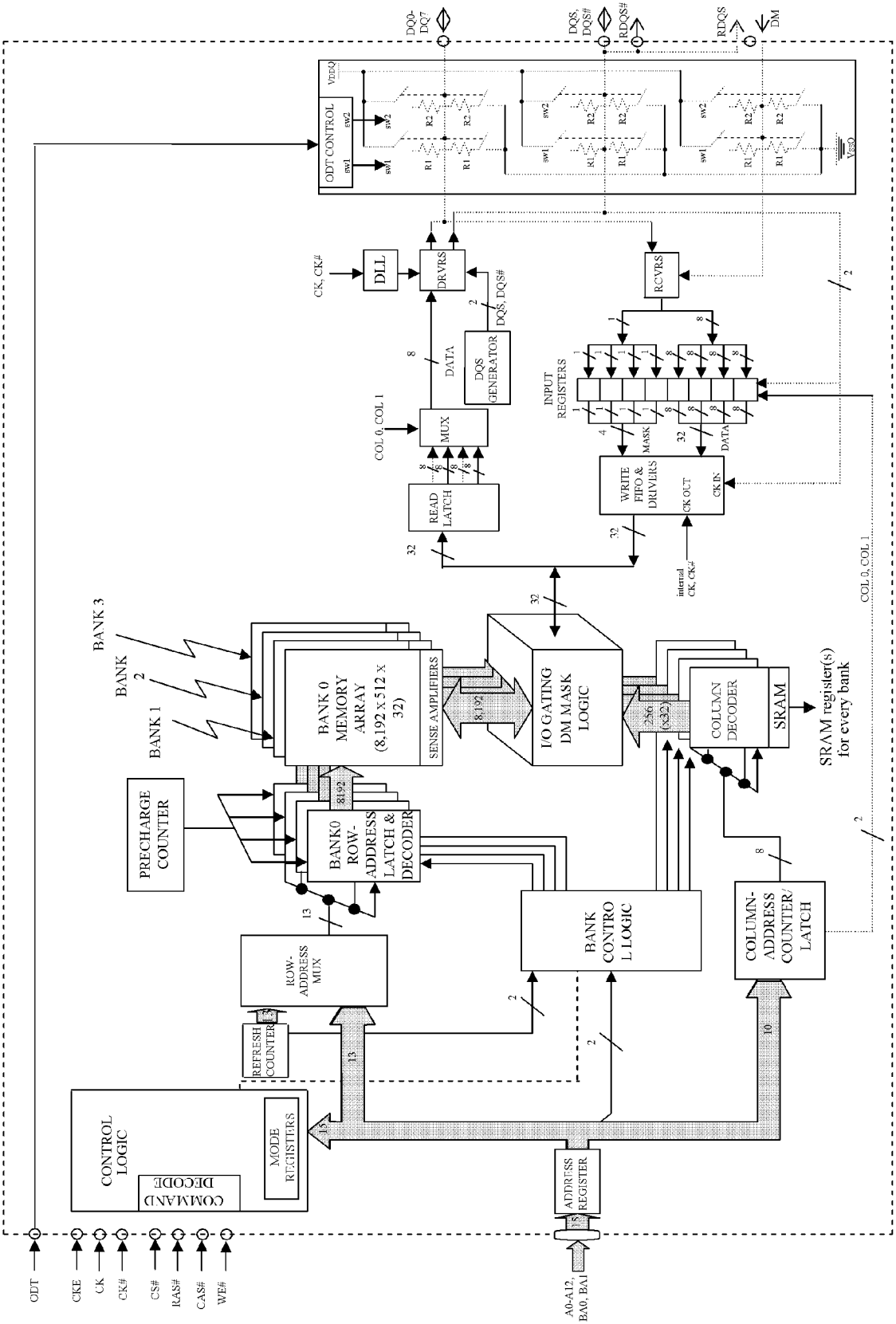

ODT
CKE
CK
CK#
CS#
RAS#
CAS#
WE#
A0-A12, BA0, BA1
CONTROL LOGIC
COMMAND DECODE
MODE REGISTERS
REFRESH COUNTER
ROW-ADDRESS MUX
ADDRESS REGISTER
PRECHARGE COUNTER
BANK 3
BANK 2
BANK 1
BANK 0 MEMORY ARRAY (8,192 x 512 x 32)
SENSE AMPLIFIERS
BANK0 ROW-ADDRESS LATCH & DECODER
I/O GATING DM MASK LOGIC
BANK CONTROL LOGIC
COLUMN DECODER
SRAM
SRAM register(s) for every bank
COLUMN-ADDRESS COUNTER/ LATCH
COL 0, COL 1
READ LATCH
MUX
DATA
DQS GENERATOR
DLL
DRVRS
RCVRS
CK, CK#
DQS, DQS#
INPUT REGISTERS
MASK
DATA
WRITE FIFO & DRIVERS
CK OUT
CK IN
internal CK, CK#
ODT CONTROL
VDDQ
VSSQ
DQ0-DQ7
DQS, DQS#
RDQS#
RDQS
DM

FIGURE 9

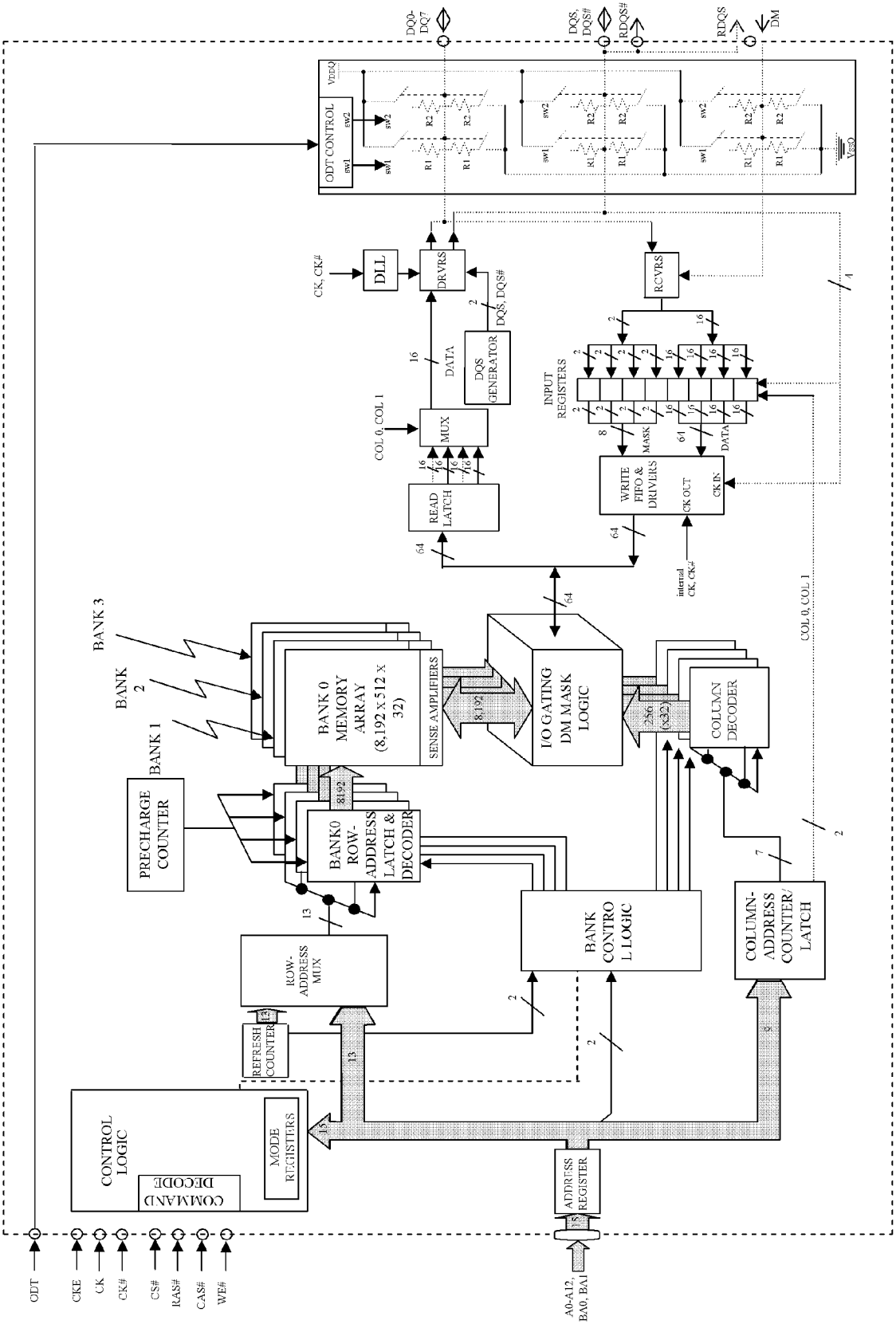
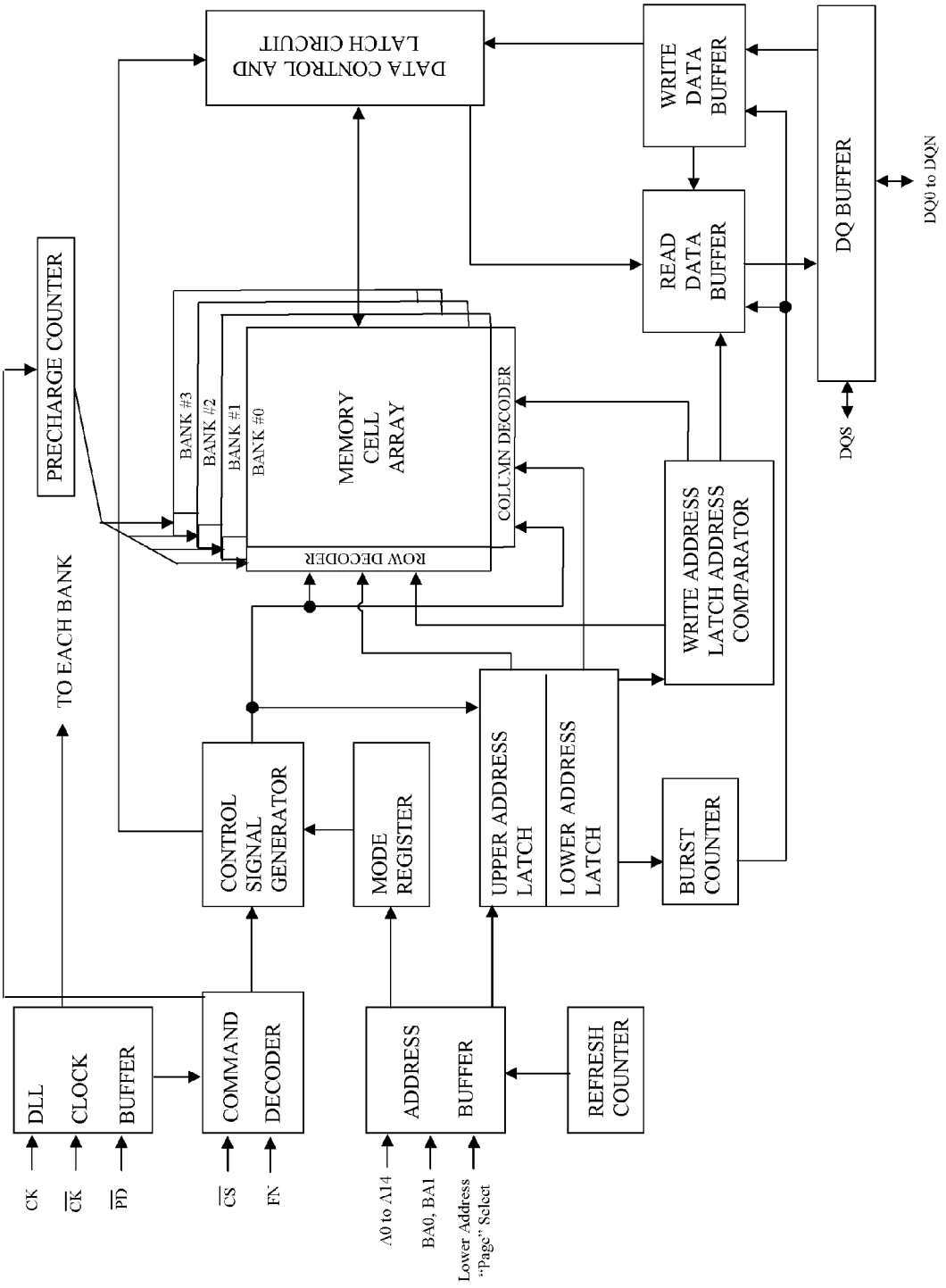

ODT
CKE
CK
CK#
CS#
RAS#
CAS#
WE#
A0-A12, BA0, BA1
CONTROL LOGIC
COMMAND DECODE
MODE REGISTERS
REFRESH COUNTER
ROW-ADDRESS MUX
ADDRESS REGISTER
BANK CONTROL LOGIC
COLUMN-ADDRESS COUNTER/ LATCH
PRECHARGE COUNTER
BANK0 ROW-ADDRESS LATCH & DECODER
BANK 0 MEMORY ARRAY (8,192 x 512 x 32)
SENSE AMPLIFIERS
I/O GATING DM MASK LOGIC
COLUMN DECODER
BANK 3
BANK 2
BANK 1
COL 0, COL 1
READ LATCH
MUX
DATA
DQS GENERATOR
DRVRS
DLL
CK, CK#
DQS, DQS#
WRITE FIFO & DRIVERS
CK OUT
CK IN
internal CK, CK#
INPUT REGISTERS
MASK
DATA
RCVRS
ODT CONTROL
VDDQ
VSSQ
DQ0-DQ7
DQS, DQS#
RDQS#
RDQS
DM

FIGURE 10


CK
$\overline{CK}$
$\overline{PD}$
$\overline{CS}$
FN
A0 to A14
BA0, BA1
Lower Address "Page" Select
DLL
CLOCK
BUFFER
COMMAND
DECODER
ADDRESS
BUFFER
REFRESH
COUNTER
CONTROL
SIGNAL
GENERATOR
MODE
REGISTER
UPPER ADDRESS
LATCH
LOWER ADDRESS
LATCH
BURST
COUNTER
WRITE ADDRESS
LATCH ADDRESS
COMPARATOR
TO EACH BANK
PRECHARGE COUNTER
BANK #3
BANK #2
BANK #1
BANK #0
MEMORY
CELL
ARRAY
ROW DECODER
COLUMN DECODER
DATA CONTROL AND
LATCH CIRCUIT
READ
DATA
BUFFER
WRITE
DATA
BUFFER
DQ BUFFER
DQS
DQ0 to DQN

Burst Read with Auto Precharge (JEDEC Standard DDR2 DRAM Specification, September 2003)

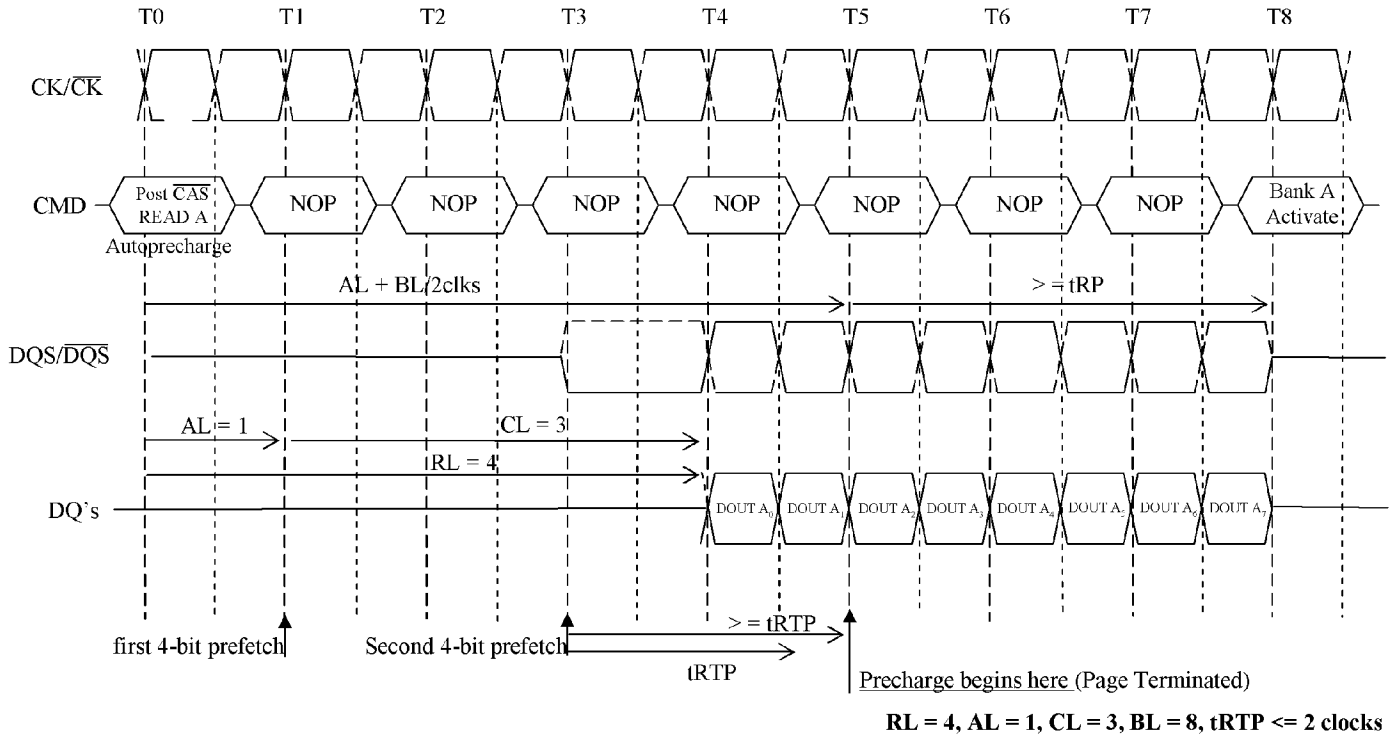


FIGURE 11

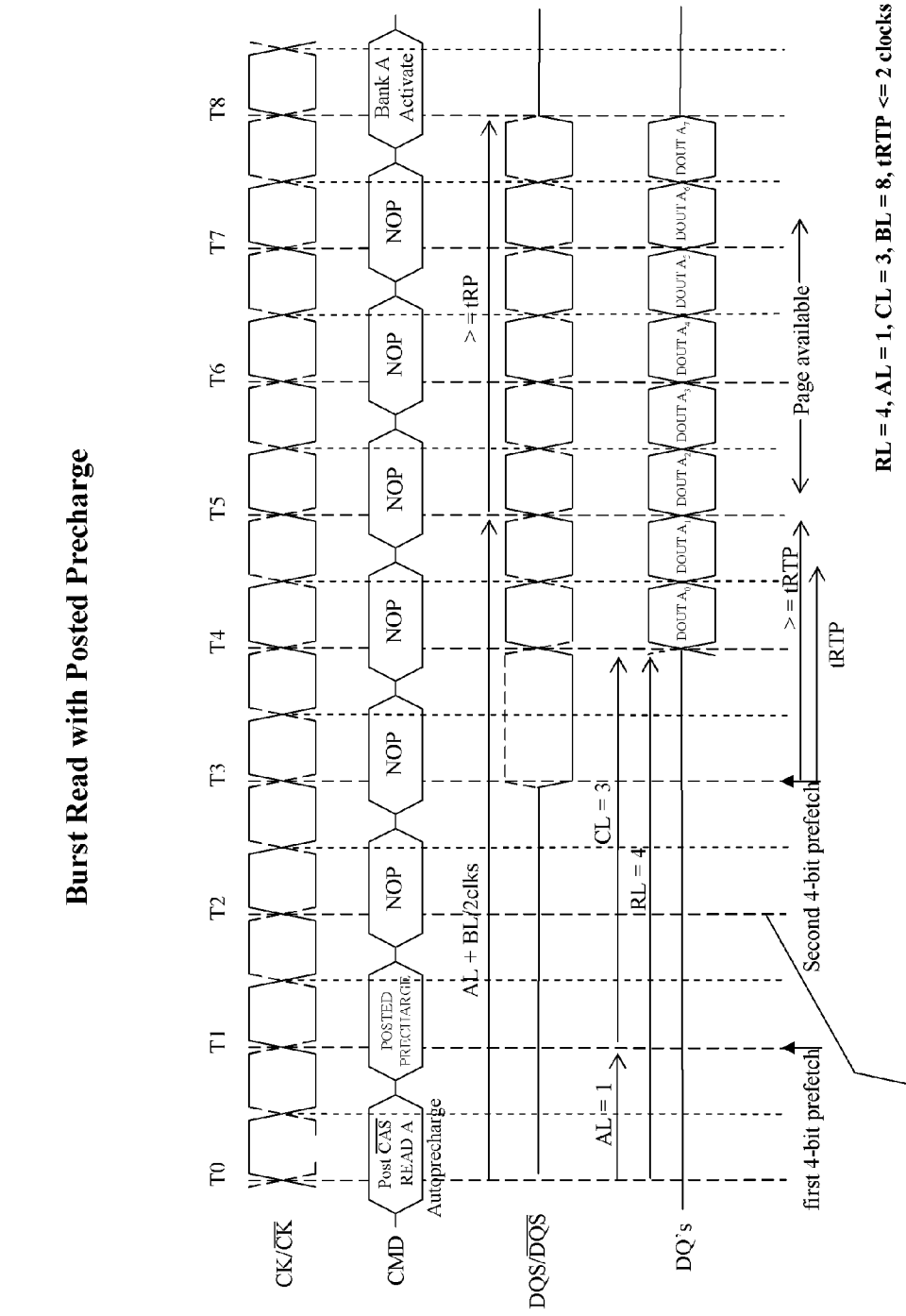

Burst Read with Posted Precharge
T0
T1
T2
T3
T4
T5
T6
T7
T8
CK/CK
CMD
Post CAS READ A
POSTED PRECHARGE
NOP
Bank A Activate
Autoprecharge
AL + BL/2clks
>= tRP
DQS/DQS
AL = 1
CL = 3
tRL = 4
DQ's
DOUT A0
DOUT A1
DOUT A2
DOUT A3
DOUT A4
DOUT A5
DOUT A6
DOUT A7
first 4-bit prefetch
Second 4-bit prefetch
>= tRTP
tRTP
Page available
RL = 4, AL = 1, CL = 3, BL = 8, tRTP <= 2 clocks
Internal Precharge (Programmable) enable activated

FIGURE 12